These are sample MCQs to indicate pattern, may or may not appear in examination

Mahatma Education Society's
Pillai HOC College of Engineering and Technology

Program: BE Electronics Engineering
Curriculum Scheme: Revised 2016
Examination: BE SEM VIII
Course Code: ELX802 and Course Name: Analog & Mixed VLSI Design

Time: 1hour Max. Marks: 50

Note to the students:- All the Questions are compulsory and carry equal marks .

Q	How to solve start up problem of supply independent biasing?	M
A	By adding diode connected device	1
A	By adding additional current mirror circuit	0
A	By adding resistor in path	0
A	By adding cascode in path	0
Q	What is disadvantage of supply independent biasing?	M
A	it is not denpends on supply voltage	0
A	it is denpends on process and temperature	1
A	it is denpends on humidity and temperature	0
A	it is bulty circuit	0
Q	Why PMOS device suffer from lower current drive capability?	M
A	conductivity of holes is less than conductivity of electron	0
A	speed of holes is less than speed of electron	0
A	Mobility of holes is less than mobility of electron	1
A	Mobility of holes is more than mobility of electron	0
Q	To avoid body effect in NMOS device select method to implement in ci	M

A	Provide P well to NMOS device	0
A	Provide Shield to NMOS device	0
A	Connect N substrate to Ground	0
A	Connect P substrate to Ground	1
Q	identify circuit in which current mirror is placed in load condition of c	M
A	Passive current mirror circuit	0
A	Active current mirror circuit	0
A	diffentiial amplifier with current mirror	1
A	Balance current mirror circuit	0
Q	Select advantage of cascode current mirror circuit over simple curren	M
A	reduce punch through effect	0
A	More head room is required	0
A	channel length modulation effect can be overcome	1
A	high current boosting	0
Q	In MOS small signal model body effect of device is represent by	M
A	gmb.Vbs	1
A	gmb.Vds	0
A	gm.Vgs	0
A	gmb.Ids	0
Q	Identify material which is used for making gate	M
A	sio2	0
A	N type Si	0
A	P typa Si	0
A	Polysilicon+metal	1
Q	Differential Amplifier has_____value of CMRR	M
A	High	1
A	Low	0
A	1	0
A	0	0
Q	The tail current in a differential amplifier equal ___	M
A	difference between two source currents	0
A	sum of two source currents	1

A	drain current divided by current gain	0
A	drain voltage divided by drain resistance	0
Q	Ideally common-mode voltage gain of differential amplifier is _____	M
A	high	1
A	very low	0
A	1	0
A	zero	0
Q	When a differential amplifier is operated as single-ended?	M
A	the output is grounded	0
A	one input is grounded and signal is applied to the other	1
A	both inputs are connected together	0
A	the output is not inverted	0
Q	The average power of flicker noise depends on:	M
A	Thickness of oxide	0
A	Voltage on oxide	0
A	Length of channel	0
A	Cleanness of the oxide silicon interface	1
Q	Thermal noise current in the MOSFET is proportional to:	M
A	Transconductance	1
A	Resistance	0
A	Gate voltage	0
A	Drain Voltages	0
Q	Which of the following is true?	M
A	Folded cascode amplifier is a single-pole operational amplifier with la	1
A	Folded cascode amplifier is a dual-pole operational amplifier with larg	0
A	Folded cascode amplifier is a single-pole operational amplifier with sr	0
A	Folded cascode amplifier is a single-pole operational amplifier with la	0
Q	The maximum and minimum output voltage of the Differential amplifi	M
A	Vmax = VDD, Vmin = -VDD	0
A	Vmax = VDD, Vmin = Rd.Iss	0
A	Vmax = VDD, Vmin = VDD – Rd.Iss	1
A	Cannot be determined	0
Q	What is telescopic Op-Amp?	M

A	To achieve high gain differential cascode topologies are used	1
A	To achieve small gain differential cascode topologies are used	0
A	To achieve high impedance differential cascode topologies are used	0
A	To achieve small impedance differential cascode topologies are used	0
Q	The output voltage of open loop opamp is always equal to ____.	M
A	supply voltage value	1
A	zero	0
A	1	0
A	infinite	0
Q	The phase response of OP amp is the graph of	M
A	phase verses frequency	1
A	phase verses magnitude	0
A	phase verses phase	0
A	None of the options	0
Q	The ideal Op – Amp has the following characteristics.	M
A	Ri = ∞, A = ∞, R0 = 0	1
A	Ri = 0, A = ∞, R0 = 0	0
A	Ri = ∞, A = ∞, R0 = ∞	0
A	Ri = 0, A = ∞, R0 = ∞	0
Q	An ideal op-amp is an ideal	M
A	voltage controlled current source	0
A	voltage controlled voltage source	1
A	current controlled current source	0
A	current controlled voltage source	0
Q	Gain of Noninverting Amplifier will be	M
A	1+(Rf/R1)	1
A	1	0
A	Rf/R1	0
A	0	0
Q	In ideal voltage-controlled oscillator, the output frequency is _____fu	M
A	Linear	1
A	Non linear	0
A	Exponential	0

A	Gaussian	0
Q	The oscillating frequency of an N-Stage ring is equal to _____ (Td de	M
A	2NTd	0
A	1/(2NTd)	1
A	2N/Td	0
A	N/2Td	0
Q	In Charge pump PLL charge pump consists of _____switched source	M
A	One	0
A	Two	1
A	Three	0
A	Four	0
Q	The _____incorporates a voltage-controlled delay line rather than	M
A	PLL	0
A	CPLL	0
A	DLL	1
A	PD	0
Q	What is longform of AMS design flow?	M
A	Analog Mixed Signal design	1
A	Analog Module Signal Design	0
A	Antenna Mixed Signal Design	0
A	None of the options	0
Q	In CMOS technologies, modified for analog design _____ are fabricate	M
A	Resistor	0
A	Capacitor	1
A	wire	0
A	inductor	0
Q	The wide transistors are usually _____ so as to reduce both the	M
A	folded	1
A	unfolded	0
A	twisted	0
A	maintained	0
Q	The low resistivity of the substrate creates unwanted paths between v	M
A	Substrate coupling	1

A	source coupling	0
A	drain coupling	0
A	gate coupling	0
Q	Which of the following option is **not true** ?	M
A	Comparator compares input signal levels	0
A	Switch capacitor integrator consist of combination of switches & capa	0
A	noninverting amplifier has same polarity as input voltage signal	0
A	Switch capacitor circuit is more sensitive towards parasitics	1
Q	Which of the following option is **true** ?	M
A	Use Unity gain buffer in sample and hold circuit provides fast charging	1
A	Use Unity gain buffer in sample and hold circuit provides slow chargir	0
A	Use Unity gain buffer in sample and hold circuit provides fast charging	0
A	Use Unity gain buffer in sample and hold circuit provides slow chargir	0
Q	Which of the following option is **not true** ?	M
A	noninverting amplifier has same polarity as input voltage signal	0
A	Switch capacitor circuit is more insensitive towards parasitics	0
A	Switch capacitor integrator consist of combination of switches & capa	0
A	Use Unity gain buffer in sample and hold circuit provides fast charging	1
Q	What is advantage of adaptive biasing?	M
A	It reduces power dissipation of circuit	1
A	It increases power dissipation of circuit	0
A	power dissipation of circuit remains constant	0
A	it reduces output current driving capability	0
Q	Adaptive biasing_____the power dissipation of VLSI circuit	M
A	reduces	1
A	increases	0
A	double	0
A	unchanged	0
Q	Adapting biasing of VLSI circuits _____output current drive ca	M
A	increases	1
A	decreases	0
A	half	0
A	unchanged	0
Q	Which of the following adds nonlinearity to analog multipliers?	M

A	Multiple multiplier stage	0
A	gain stage	0
A	offset reduction	0
A	inherent offset voltage	1
Q	Which of the following makes analog multipliers more linear?	M
A	Multiple multiplier stage	0
A	gain stage	0
A	offset reduction	1
A	inherent offset voltage	0
Q	Error band in a MOSFET switch should be	M
A	50%	0
A	100%	0
A	high	0
A	low	1
Q	Time constant of a MOSFET switch is	M
A	RonC	1
A	LC	0
A	RL	0
A	1.2RC	0
Q	The equation Qch=WLCox(VDD-Vin-Vth) represents	M
A	channel charge	1
A	Oxide charge	0
A	substrate charge	0
A	None of the options	0
Q	The equation sqrt(KT/C) is ____	M
A	inductance	0
A	resistance	0
A	rms value of total noise current	0
A	rms value of total noise voltage	1
Q	How many control lines are present in analog to digital converter in a	M
A	Three	0
A	Two	1
A	One	0

A	Four	0
Q	Find out the integrating type analog to digital converter?	M
A	Flash type converter	0
A	Tracking converter	0
A	Counter type converter	0
A	Dual slope ADC	1
Q	Which A/D converter is considered to be simplest, fastest and most ex	M
A	Servo converter	0
A	Counter type ADC	0
A	Flash type ADC	1
A	Cyclic DAC	0
Q	The flash type A/D converters are called as	M
A	Parallel non-inverting A/D converter	0
A	Parallel counter A/D converter	0
A	Parallel inverting A/D converter	0
A	Parallel comparator A/D converter	1
Q	The number of comparator required for flash type A/D converter	M
A	Triples for each added bit	0
A	Reduce by half for each added bit	0
A	Double for each added bit	1
A	Doubles exponentially for each added bit	0
Q	Calculate the conversion time of a 12-bit counter type ADC with 1MHz	M
A	4.095 μs	0
A	4.095ms	1
A	4.095s	0
A	4.095ns	0
Q	In a servo tracking A/D converter, the input voltage is greater than the	M
A	The counter count up	1
A	The counter count down	0
A	The counter back and forth	0
A	Fast Counting	0
Q	At what condition error occurs in the servo tracking A/D Converter?	M
A	Slow change input	0
A	Rapid change in input	1

A	No change in input	0
A	Random input change	0